WHAT IS CLAIMED IS:

1. A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof; and

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit through a bus switch on said printed circuit board.

2. The method of Claim 1, wherein the memory integrated circuit comprises synchronous DRAM.

3. The method of Claim 1, interfacing a state decoder with the bus switch.

4. The method of Claim 3, wherein the stated decoder is structured to decode at least one control gate and control the bus switch in response thereto.

5. A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof; and

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit; and

positioning a switch in a data path to the memory integrated circuit

6. The method of Claim 1, wherein the memory integrated circuit comprises synchronous DRAM.

7. The method of Claim 1, additionally comprising interfacing a state decoder with the bus switch.

8. The method of Claim 3, wherein the stated decoder is structured to decode at least one control gate and control the bus switch in response thereto.

9. The method of Claim 5, wherein the memory integrated circuit comprises the switch.

10. The method of Claim 5, wherein the bus switch is positioned externally with respect to the memory integrated circuit.

11. A method of making a memory integrated circuit comprising the acts of:

connecting data input terminals to an input portion of a bus switch;

connecting an output portion of said bus switch to a data input buffer; and

coupling an output of said data input buffer to a memory storage circuit.

12. A method of data transfer across a bus comprising the acts of:

reducing the parasitic capacitance of said bus by isolating at least a first segment of said bus; and

utilizing a second segment of said bus for data transfer.